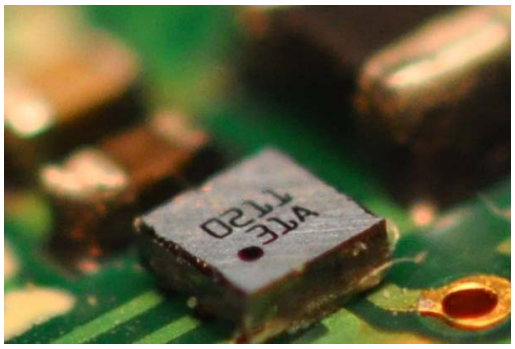
PM3110

High efficiency step-down DC/DC regulator for 3G HSUPA, LTE application

Final Data

Features

- Regulated output: 0.6 – 3.6 V corresponding to VCTRL = 0.24 – 1.44 V
- More than 650 mA load capability
- High efficiency: up to 95% entire device
- Pulse Skipping (PSK) mode to optimize the efficiency at low/medium WCDMA power level
- 2.5 V to 4.8 V battery input range
- Internal synchronous switch
- PWM switching frequency 3.2 MHz
- Shutdown mode (EN pin)
- Bypass mode (100% duty cycle)
- Small WLCSP (1.2 mm x 1.2 mm) package



WLSCP 1.2 mm x1.2 mm x 0.6 mm
with nine balls and 0.4 mm pitch

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Applications

- W-CDMA, CDMA, TD-SCDMA, LTE modems
- Mobile phones
- Portable instruments
- PDAs and hand held terminals

Description

The PM3110 is a step-down DC-DC monolithic switching regulator using 3.2 MHz switching frequency. The output voltage is determined by a variable control voltage on the input pin VCTRL. Synchronous rectification and Pulse Skipping are used to improve efficiency. The user can prohibit the Pulse Skipping Mode via the MODE pin and thus force pure PWM operation mode. An internal free running oscillator generates the clock of the DC-DC.

Content

1 Pin description

Figure 1 and *Figure 2* show PM3110 package top and bottom views. The 9-ball WLSCP package dimensions are 1.2 mm x 1.2 mm x 0.6 mm with 0.4 mm pitch.

Figure 1. WLSCP top view

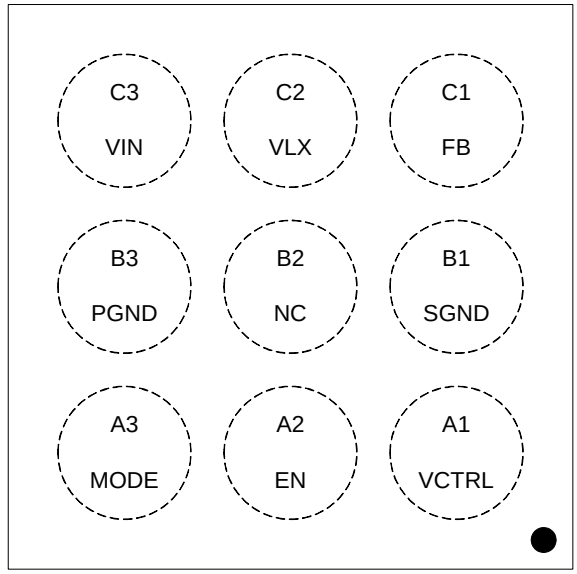


Figure 2. WLSCP bottom view

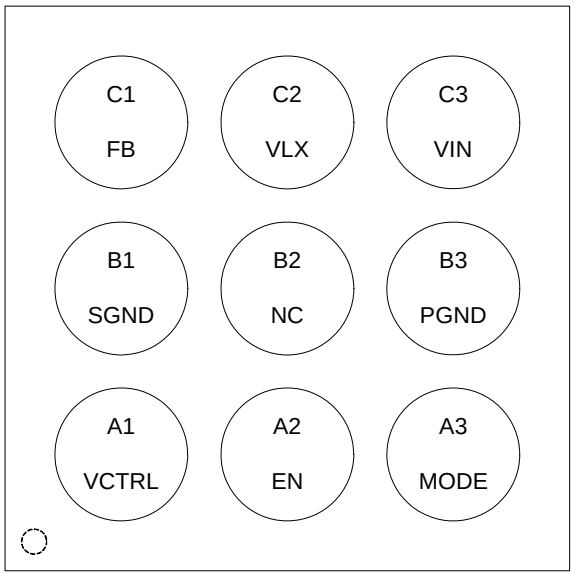


Table 1. PM3110 pin functions (WLSCP package)

Pin number	Symbol	Description
A1	VCTRL	Reference voltage input
A2	EN	EN = High to enable the device EN = Low to disable the device Do not let high impedance
A3	MODE	MODE= High to enable the Pulse Skipping Mode MODE= Low to force the pure PWM operation mode Do not let high impedance
B1	SGND	Signal ground pin
B2	NC	Not connected, do not connect
B3	PGND	Power ground pin
C1	FB	Feedback pin
C2	VLX	Power stage output
C3	VIN	Supply voltage input

2 Operation description

2.1 Shutdown mode / reset

When EN='0', the circuit is disabled. VLX node is shorted to ground through a pull-down resistor. To ensure minimal consumption, inputs EN, MODE and VCTRL should be at zero level. In this case, consumption on VIN is less than µA.

2.2 Startup sequence / slope control

When EN rises to '1' the circuit internally starts its operation. Once the internal oscillator frequency stabilizes and all blocks are correctly biased, the power stage is enabled and the output voltage starts rising. This delay between EN='1' and the first edge of VLX is typically 20µs.

PM3110 implements a startup circuit which controls the slope of the output voltage. This startup technique combines the advantage of limiting the inrush current while maintaining stable operation, which is not the case when startup relies on current limitation. Inrush current with no load can be calculated by the following formula:

$$I_{INRUSH} = C_{LOAD} \cdot SR$$

SR being the controlled Slew Rate. The slew rate has been designed not to generate an IINRUSH such as the current limitation circuit would trigger with no load while fitting with thigh timings. The startup sequence is finished when the output voltage has reached VCTRL*2.5. It is recommended to set VCTRL before raising the enable signal.

2.3 Voltage transitions

Voltage transitions are important when supplying a WCDMA PA. In PM3110, they are performed using the Slope Control circuit described in previous paragraph. When user changes the value of VCTRL either up or down, the output voltage rises or falls with given slew rate SR. It has to be noted that if the sum of load current and current needed for the transition is higher than the current limitation threshold, circuit limitation will trigger. Inductor current during a transition is given by

$$I_{TRANSITION} = C_{LOAD} \cdot SR + I_{LOAD}$$

When the output voltage approaches the final value, it progressively bends in order to smoothly "land" on the final voltage with no overshoot.

2.4 CCM operation

Circuit operates in CCM mode if the PSK mode is disabled (MODE='0') or if the load current is higher than the PSK limit.

2.5 PSK operation

When MODE='1', PM3110, if the load current is low, automatically switches to PSK mode in order to maintain a good efficiency. In CCM mode, the inductor current can go reverse at low load. This has a very negative impact on the efficiency. In order to avoid such behavior, PM3110 implements a zero crossing comparator which detects the inversion of the current in the inductor. When the inversion is detected, the output stage goes high impedance and the inductor current remains 0 (Discontinuous Conduction Mode, DCM). From this event regulator enter in PSK mode.

The regulator maintains the output voltage by firing some fixed size pulses when needed. Between pulses output stage is in high impedance. Regulator automatically leaves this mode when current increases above the PSK threshold.

2.6 Bypass operation

PM3110 is capable of full duty cycle operation so called bypass mode. In case the requested output voltage is higher than the one physically feasible (for example VCTRL *2.5 > VBAT), the power stage continuously activate the high side MOS in order to provide the highest possible output voltage. A particular attention has been given to the transition between Full Duty Operation and normal mode.

For example, assuming that the input voltage is 3.4 V as well as the requested output voltage (VCTRL*2.5 = 3.4), the PM3110 is in Full Duty Operation. Now, imagine that the input voltage raises suddenly of 0.6 V. The voltage drop across the inductor would be 0.6 V thus dI/dt = 0.6A/µs. We can, from this figure, imagine what can be the overshoot if the regulator would have some delay (for example 2 µs) to come back to normal operation, it could easily be 500 mV.

PM3110 is able to handle this type of transition with an overshoot around 100 mV.

3 Electrical characteristics

3.1 Absolute maximum ratings

Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

Table 2. Absolute maximum ratings

Parameter	Test conditions	Min	Max.	Unit
V_{IN}	Power supply voltage	-0.3	6	V
V_{EN}	Enable input	-0.3	V_{IN}	V
V_{CTRL}	Voltage selection	-0.3	V_{IN}	V
V_{FB}	Feedback input	-0.3	V_{IN}	V
V_{LX}	Output voltage	-0.3	V_{IN}	V
T_{STG}	Storage temperature range	-55	+150	°C
ESD	HBM JESD22-A114-B and ESD STM 5.1-2001.HBM	1		kV
	CDM ANSI-ESDSTM5.3.1-1999 and JEDEC Standard JESD22-C101C	500		V

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

3.2 Recommended operating conditions

Table 3. Recommended operating conditions

Parameter	Test conditions	Min	Max.	Unit
V_{IN}	Power supply voltage	2.5	4.8	V
V_{CTRL}	Reference voltage input	0.24	1.44	V
I_{LOAD}	Load current	0	650	mA
T_A	Ambient temperature range	-40	+85	°C

3.3 Thermal data

Table 4. Thermal data

Symbol	Parameter		Value	Unit
J_A	Thermal resistance junction-ambient	WLCSP	100	°C/W

3.4 DC electrical characteristics

Characteristics measured over the recommended operating conditions unless otherwise is noted. All typical values are referred to T_A = 25°C, Vin = 3.6 V.

Table 5. DC electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{IN}	Power supply voltage		2.5		4.8	V
V_{OUT}	Output voltage	V_{CTRL} <1.44 V	0.6		3.6	V
V_{GAIN}	V_{CTRL} to V_{OUT} gain	V_{OUT} 0.6 V -3.6 V		2.5		V/V
I_{CTRL}	Control current	DC output current source/sink, R_{CTRL} = 100 kohm, C_{CTRL} = 35 pF			60	µA
R_{CTRL}	Resistive load on V_{CTRL}	Pull down resistor between VCTRL and SGND	65	100	130	kohm
C_{CTRL}	Capacitive load on V_{CTRL}			20	35	pF
V_{EN_H}	Logic high for EN		1.6			V
V_{EN_L}	Logic low for EN				0.1	V
V_{MODE_H}	Logic high for MODE		1.6			V
V_{MODE_L}	Logic low for MODE				0.1	V
R_{LX}	Pulldown res on V_{LX} when disabled	EN='0', V_{IN}=3.6V		9		ohm
Tmax	Thermal shutdown triggering limit		135	150	165	°C
Ipeak	Peak current limit in the inductor		1.2	1.6	2.1	A

3.5 AC electrical characteristics

Characteristics measured over the recommended operating conditions unless otherwise is noted. All typical values are referred to T_A = 25°C, Vin = 3.6V.

Table 6. AC electrical characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{LOAD\text{-}MAX}$	Maximum load current		650			mA
$R_{ON\text{-}PSK}$	MOS ON resistance	For V_{IN} =3.6V, PSK mode active			0.315	ohm
R_{ON}	MOS ON Resistance	For I_{LOAD} = 0.14 A, V_{IN} =3.6 V, V_{OUT} = 1.4 V			0.2	ohm
$R_{ON\text{-}FULL\text{-}DUTY}$	MOS ON Resistance	For I_{LOAD} = 0.65 A, V_{IN} =3.6V, V_{OUT} = 3.4 V			0.2	ohm
$I_{SHUTDOWN}$	Total current at shutdown	EN=0		0.1	2	µA

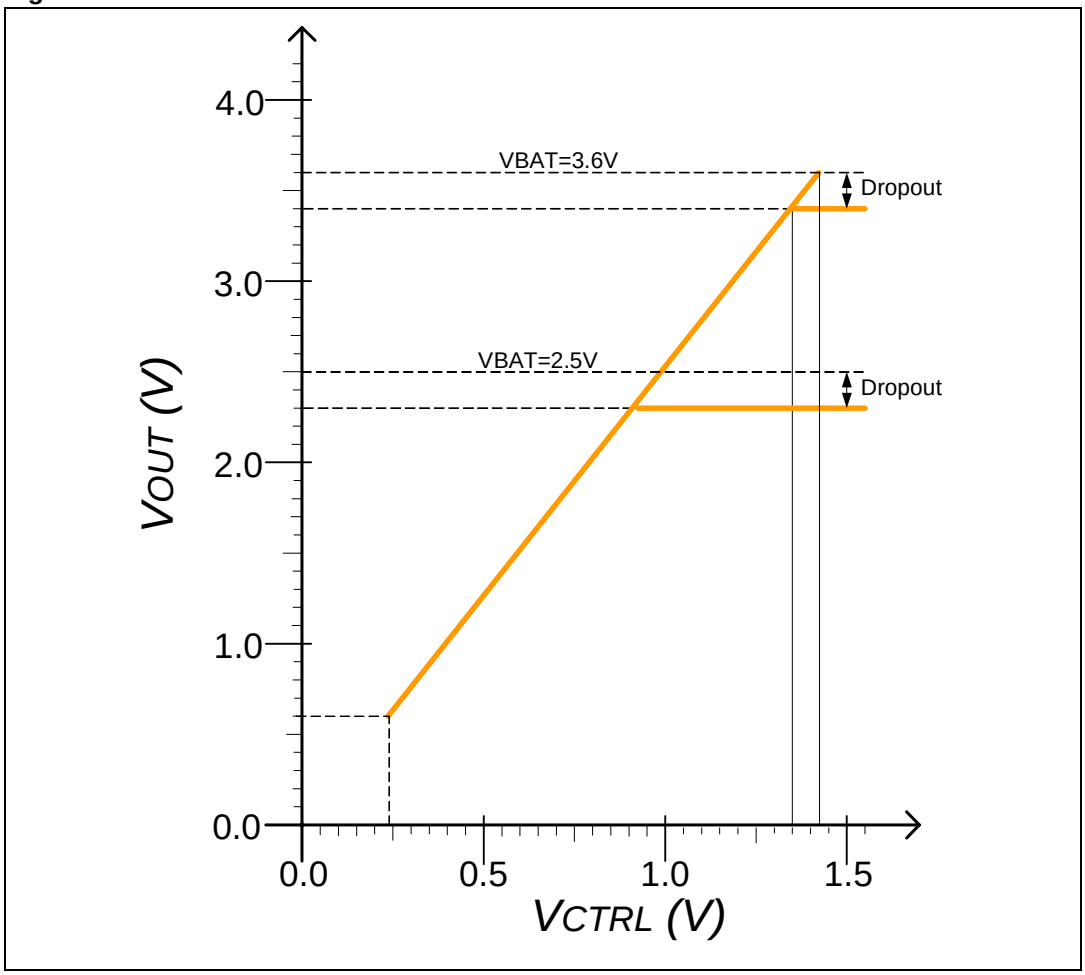
Table 6. AC electrical characteristics (continued)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{QUIESCENT}$	Quiescent current	EN=1, I_{LOAD} = 0 mA		400	600	µA
Eff	Efficiency	V_{IN} = 3.6 V V_{OUT} = 1 V, I_{OUT} = 23 mA	75	80		%
		V_{IN} = 3.6 V V_{OUT} =1.8 V, I_{OUT} = 0.15 A	85	90		%
		V_{IN} = 3.6 V V_{OUT} = 3.4 V,I_{OUT} = 0.65 A	90	95		%
f_{SW}	Switching Frequency			3.2		MHz
V_{OUT}	Output voltage accuracy	V_{CTRL}=1.36V, I_{LOAD} = 0 to 650 mA	3.37	3.4	3.43	V
		V_{CTRL}=0.32V, I_{LOAD} = 0 to 80 mA	0.775	0.8	0.825	V
V_{CTRL}	Control voltage linearity	$0.5\ V \le V_{CTRL} \le 1.2V$	-2		2	%
SR	Slew rate control during voltage transitions			0.12		V/µS
t_{SET-LH}	Voltage transition Low to High	V_{OUT} = from 0.6 V to 3.4 V I_{LOAD} = from 10 mA to 650 mA		30	50	µs
t_{SET-HL}	Voltage transition High to Low	V_{OUT} = from 3.4 V to 0.6 V I_{LOAD} = from 650 to 10 mA		30	100	µs
t_{START}	Circuit startup time	From EN='1' to V_{OUT} at nominal value $0.34\ V \le V_{CTRL} \le 1.36V$			75	µs
V_{OUT}	V_{OUT} Ripple (peak-to-peak)	I_{OUT} = 10 – 650 mA V_{OUT} = 0.6 – 3.4 V		50	100	mV

4 Typical performance characteristics

4.1 Transfer curve

Figure 3. Transfer curve



4.2 Efficiency

Figure 4. Efficiency for VOUT=0.6V

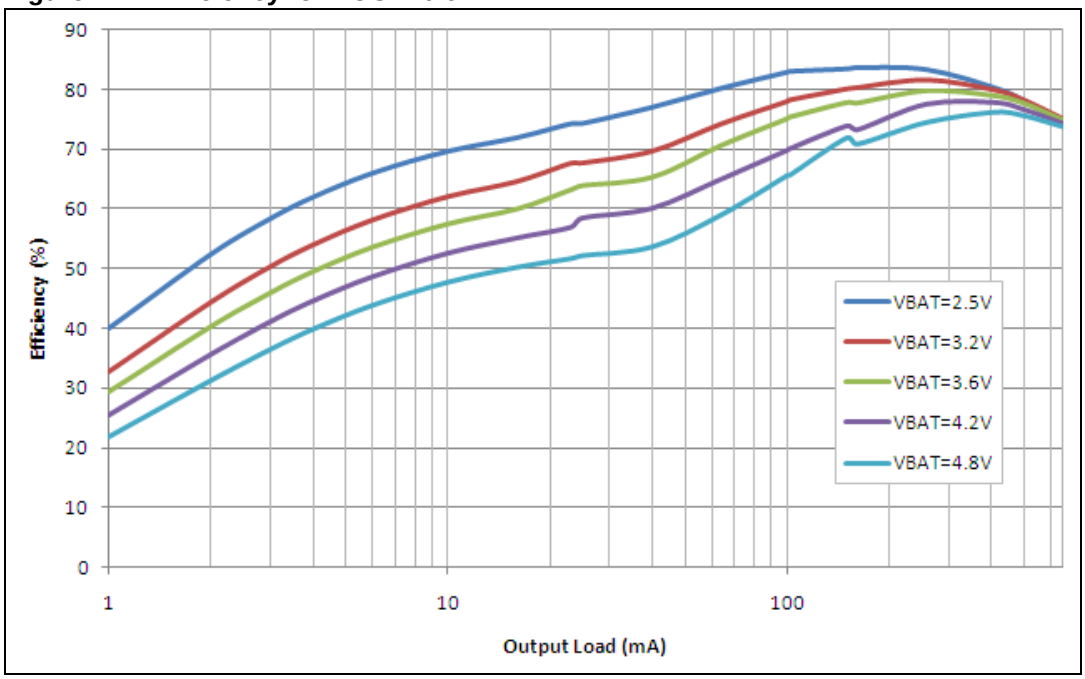


Figure 5. Efficiency for VOUT=1.2V

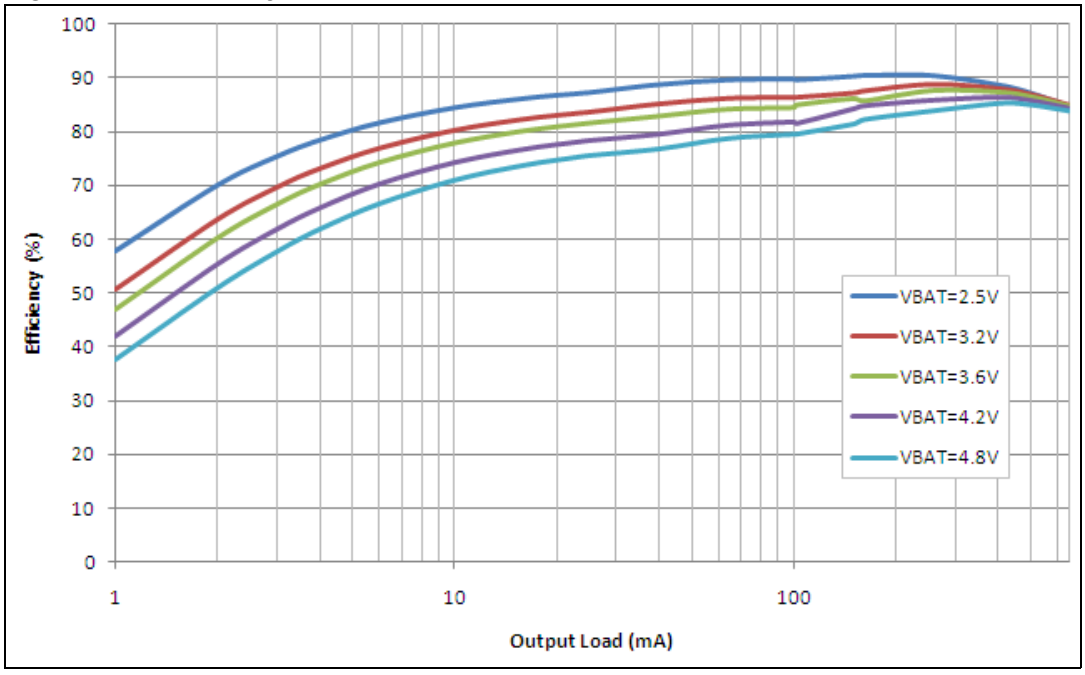


Figure 6. Efficiency for VOUT=1.8V

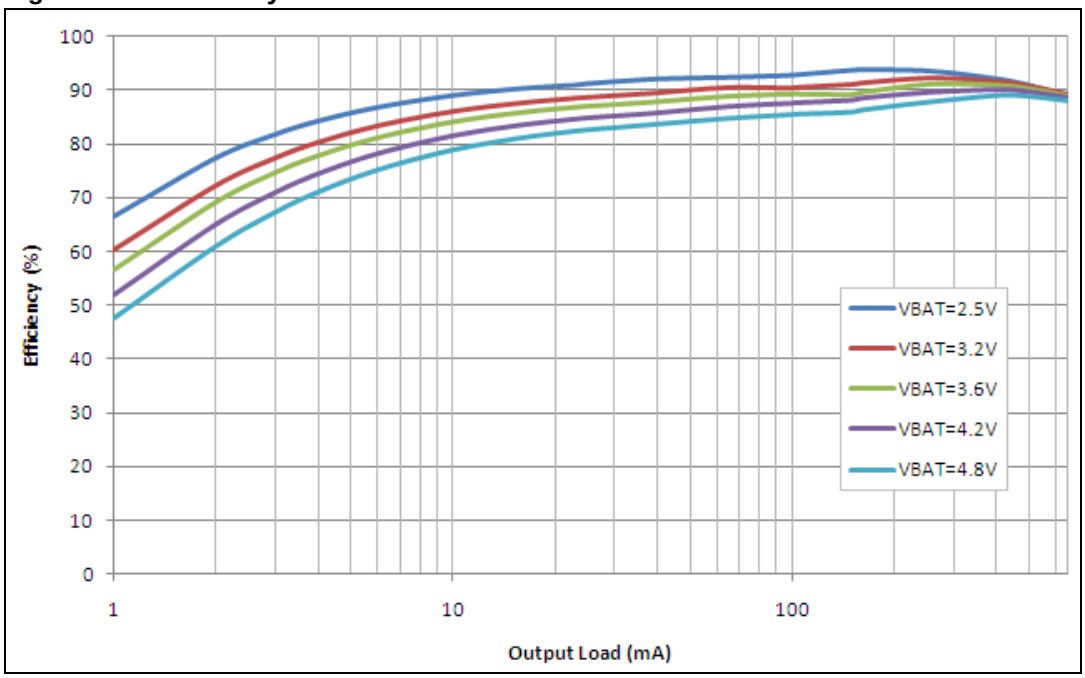


Figure 7. Efficiency for VOUT=2.4V

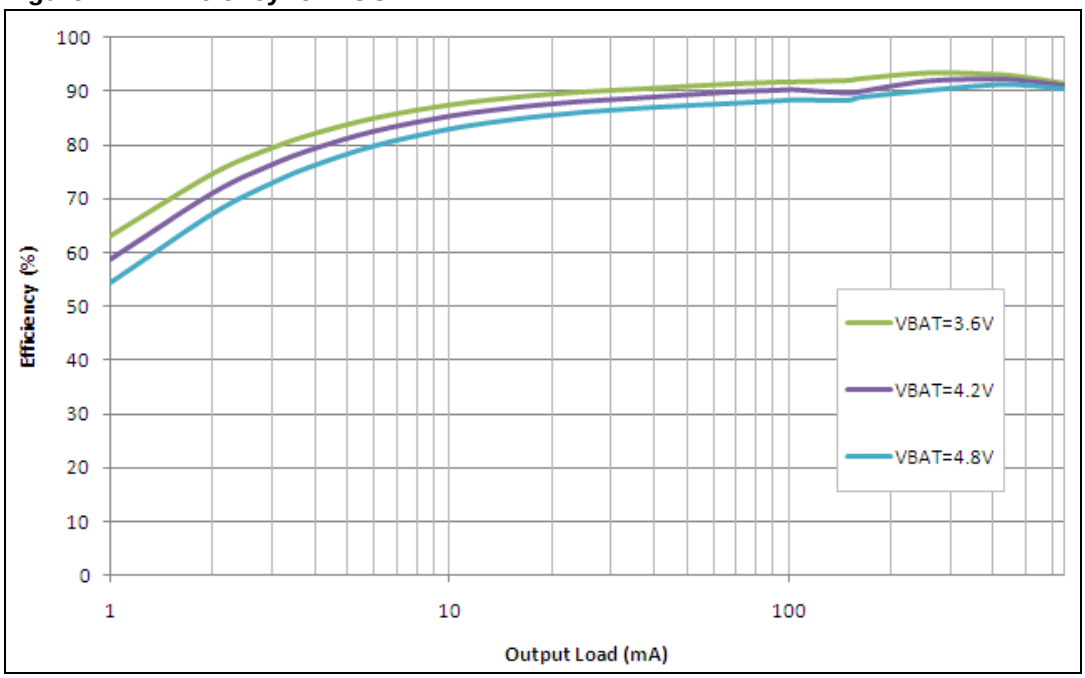


Figure 8. Efficiency for VOUT=3.1V

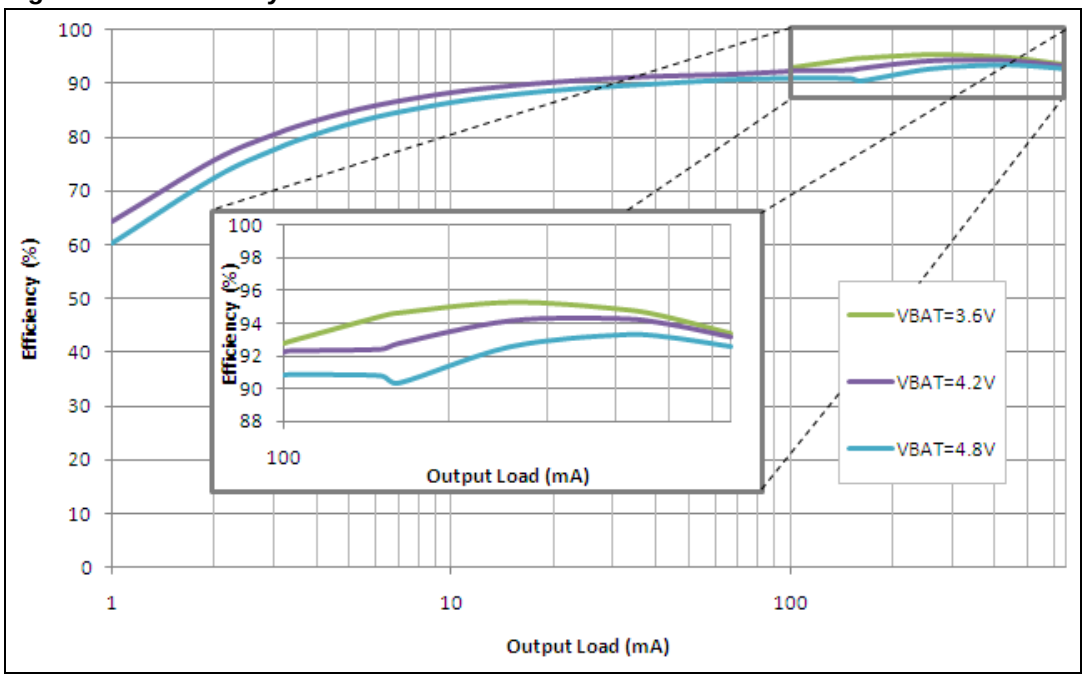
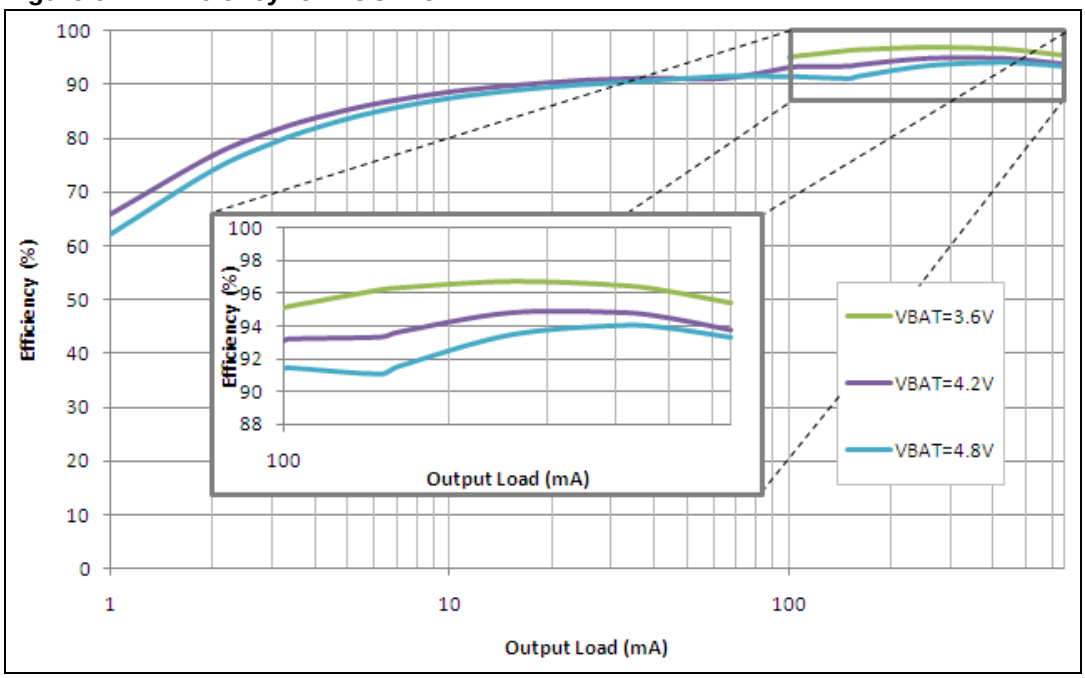
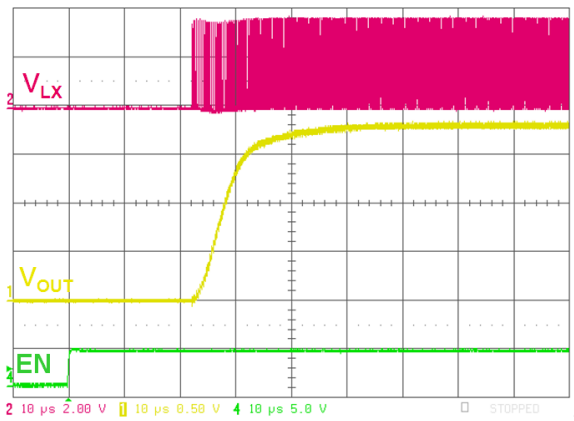


Figure 9. Efficiency for VOUT=3.4V



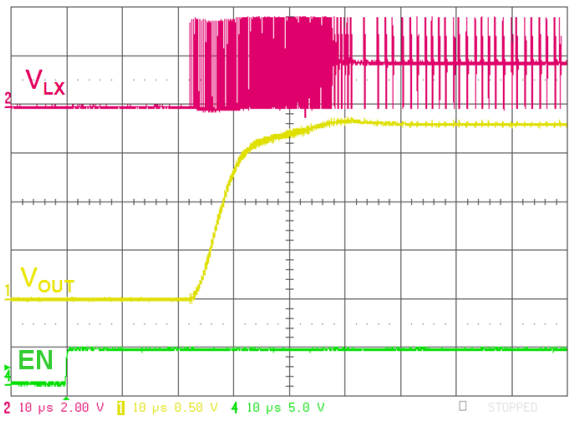
4.3 Typical operating characteristics

Figure 10. Startup sequence in CCM mode



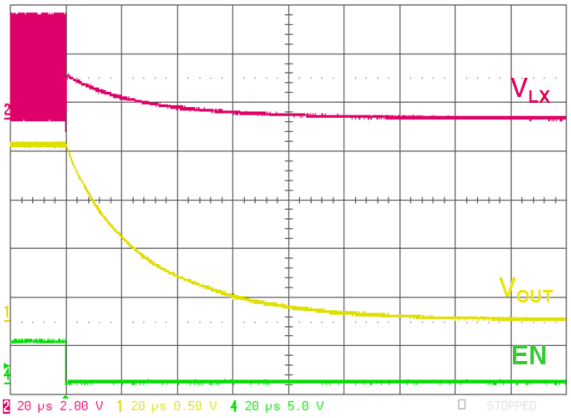
V_{IN}=3.6V, V_{OUT}=1.8V, MODE=0, R_{LOAD}=100Ω

Figure 11. Startup sequence in PSK mode



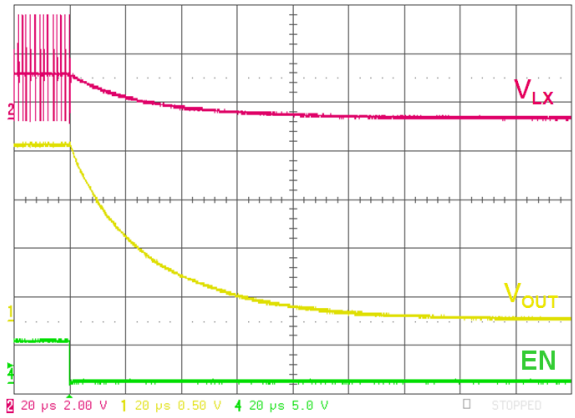
V_{IN}=3.6V, V_{OUT}=1.8V, MODE=1, R_{LOAD}=100Ω

Figure 12. Shutdown in CCM mode



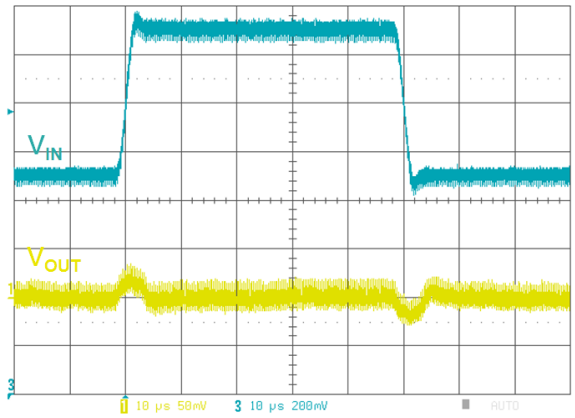
V_{IN}=4.2V, V_{OUT}=1.8V, MODE=0, R_{LOAD}=100Ω

Figure 13. Shutdown in PSK mode



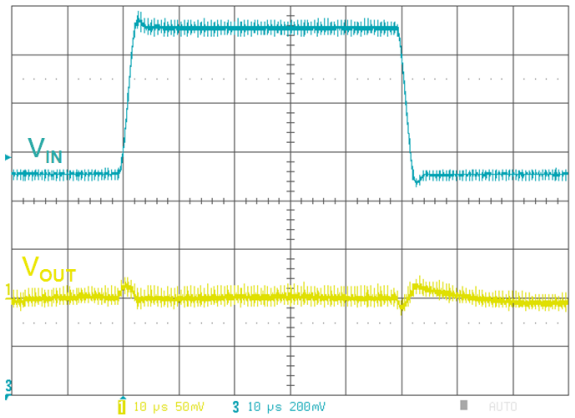
V_{IN}=4.2V, V_{OUT}=1.8V, MODE=1, R_{LOAD}=100Ω

Figure 14. Line Transient in CCM mode



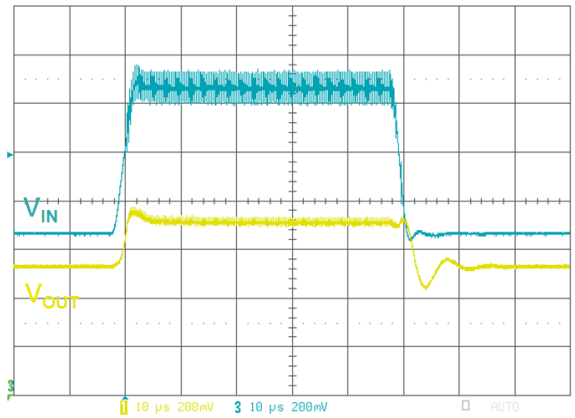
V_{IN}=3.6V to 4.2V, V_{OUT}=1.8V, MODE=1, I_{OUT}=300mA

Figure 15. Line transient in PSK mode



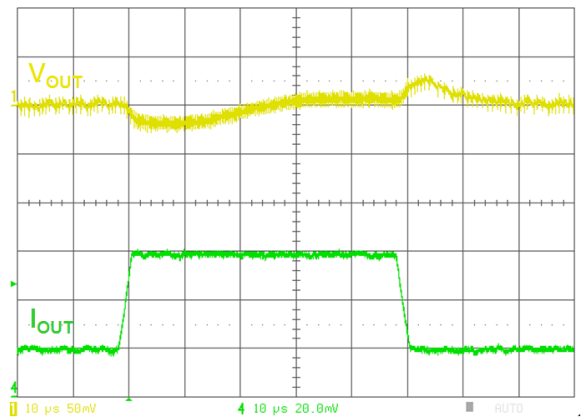
V_{IN}=3.6V to 4.2V, V_{OUT}=0.6V, MODE=1, I_{OUT}=20mA

Figure 16. Line Transient in Bypass mode



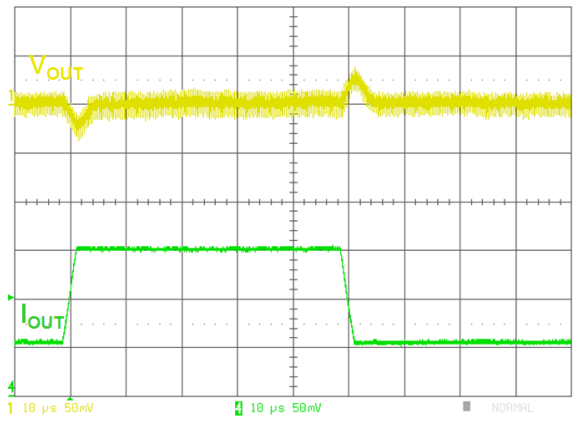
V_{IN}=3.3V to 3.8V, V_{OUT}=3.2V, MODE=0, R_{LOAD}=5.2Ω

Figure 17. Load transient in PSK mode



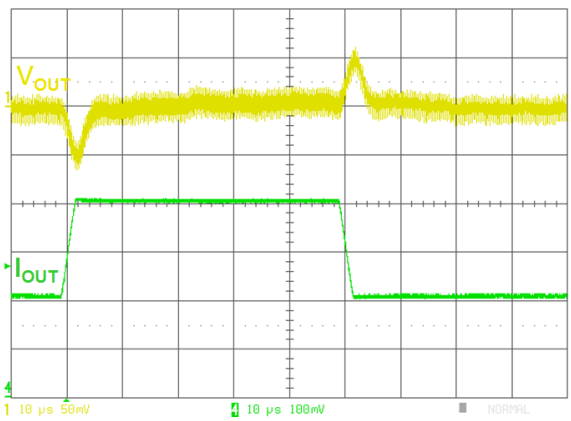
V_{IN}=3.6V, V_{OUT}=0.9V, MODE=1, I_{OUT}=20mA to 60mA

Figure 18. Load transient in CCM mode



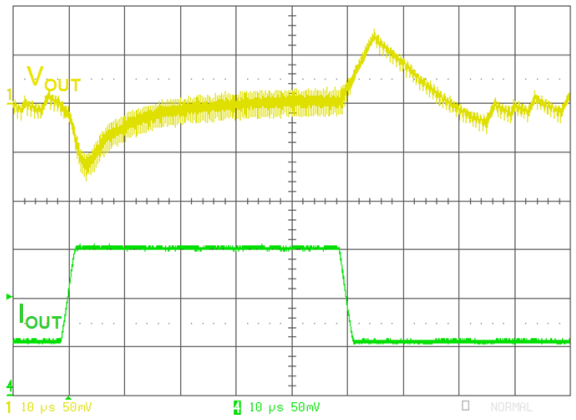
V_{IN}=3.6V, V_{OUT}=1.8V, MODE=0,
I_{OUT}=50mA to 150mA

Figure 19. Load transient in CCM mode



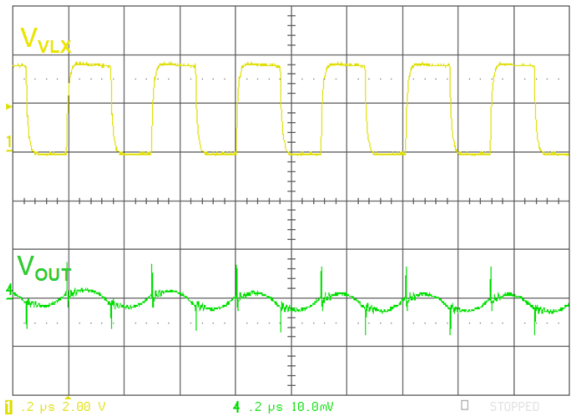
V_{IN}=3.6V, V_{OUT}=1.8V, MODE=0,
I_{OUT}=200mA to 400mA

Figure 20. Load transient in PSK mode to CCM mode



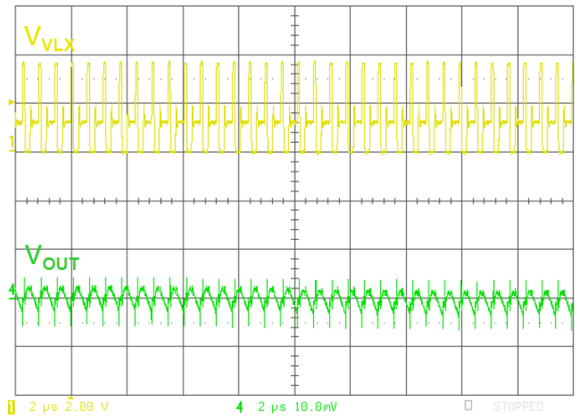
V_{IN}=3.6V, V_{OUT}=1.8V, MODE=1,
I_{OUT}=50mA to 150mA

Figure 21. Ripple in CCM mode



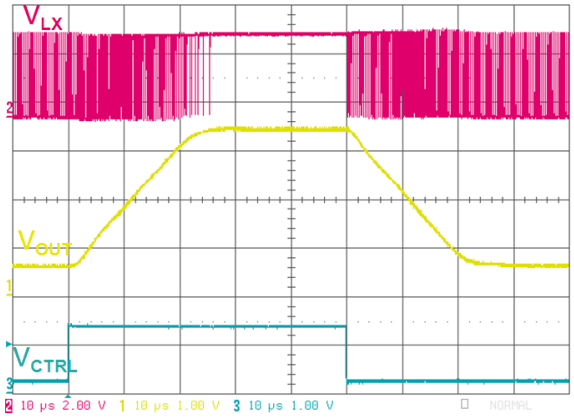
V_{IN}=3.6V, V_{OUT}=1.8V, MODE=1,
I_{OUT}=300mA

Figure 22. Ripple in PSK mode



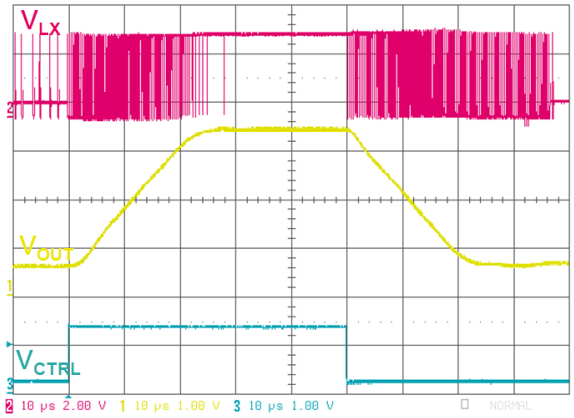
V_{IN}=3.6V, V_{OUT}=1.2V, MODE=1, I_{OUT}=40mA

Figure 23. VCTRL transient from CCM mode to Bypass mode



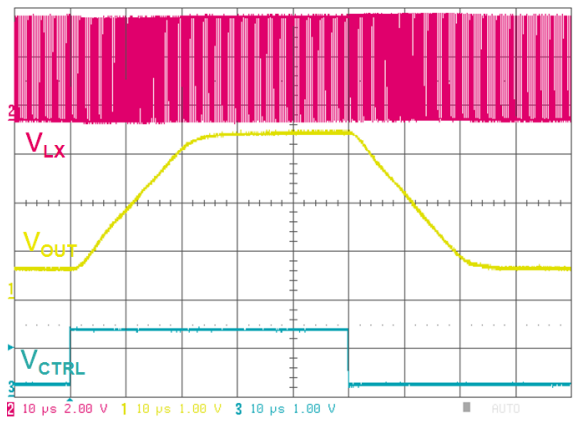
V_{IN}=3.4V, V_{OUT}=0.6V to 3.4V, MODE=0, R_{LOAD}=100Ω

Figure 24. VCTRL transient from PSK mode to Bypass mode



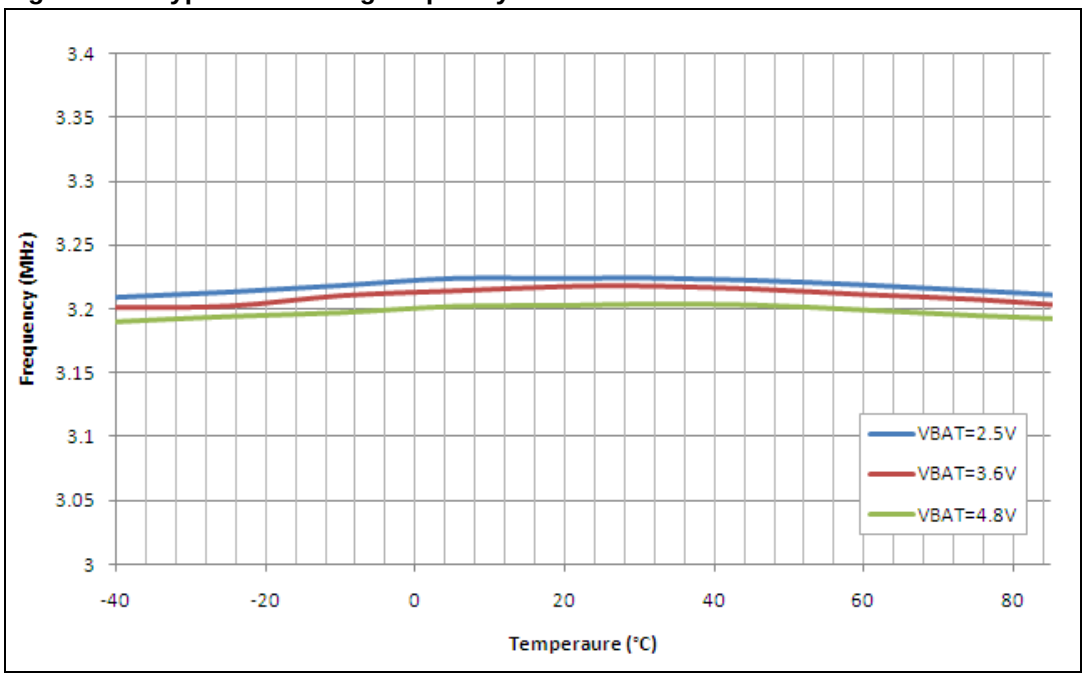
V_{IN}=3.4V, V_{OUT}=0.6V to 3.4V, MODE=1, R_{LOAD}=100Ω

Figure 25. VCTRL transient in CCM mode



V_{IN}=3.4V, V_{OUT}=0.6V to 3.4V, MODE=1, R_{LOAD}=100Ω

Figure 26. Typical switching frequency



5 Application test circuit

Figure 27. PM3110 application test circuit

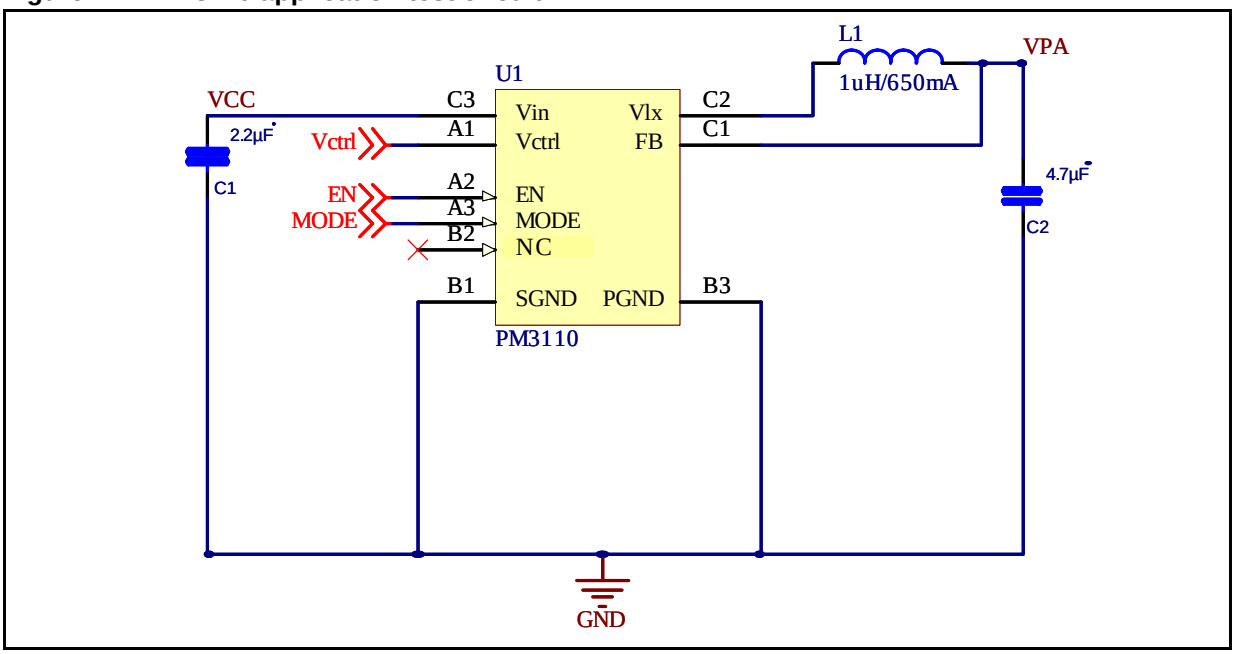


Table 7. External components specification

Parameter		Min	Typ	Max	Unit	Comments
C1	Capacitor value	1.6	2.2	2.9	µF	With all drifts included (-70%/+30%)
	Capacitor ESR	5	10	30	mΩ	Including the soldering and metal path resistance
C2	Capacitor value	1.5	4.7	6	µF	With all drifts included (-70%/+30%)
	Capacitor ESR	5	10	30	mΩ	Including the soldering and metal path resistance
L1	Inductor value	0.6	1	1.3	µH	with all drifts -40%/30%
	Inductor parasitics resistance	56	80	150	mΩ	
	Inductor rated DC current	1.2			A	

Following external components are recommended:

Table 8. Recommended external components

Component	Value	Manufacturer	Size	Manufacturer ordering Code
L1	1 µH / 1.35 A	TOKO	2.0 mm x 1.25 mm x 1.0 mm	MDT2012-CRAR0N
C2	4.7 µF / 6.3 V	muRata	0402	GRM155R60J475M
C1	2.2 µF / 6.3 V	TDK	0402	C1005X5R0J225KT

Other references can be selected as long as they respect the design limits listed in *Table 7*.

6 Recommended PCB layout

Figure 28 shows the recommended top layer and *Figure 29* shows the recommended layer 2.

Figure 28. Top layer

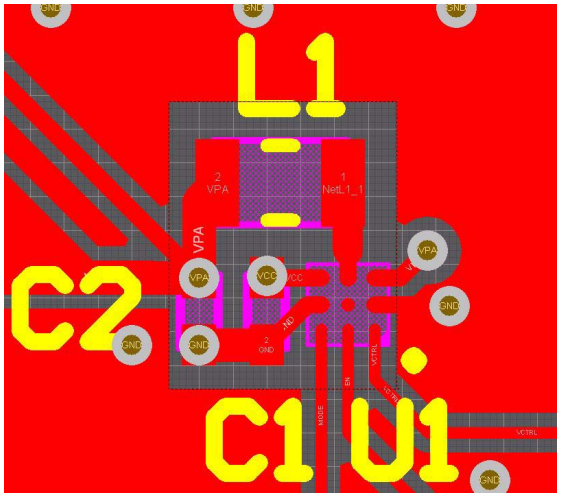
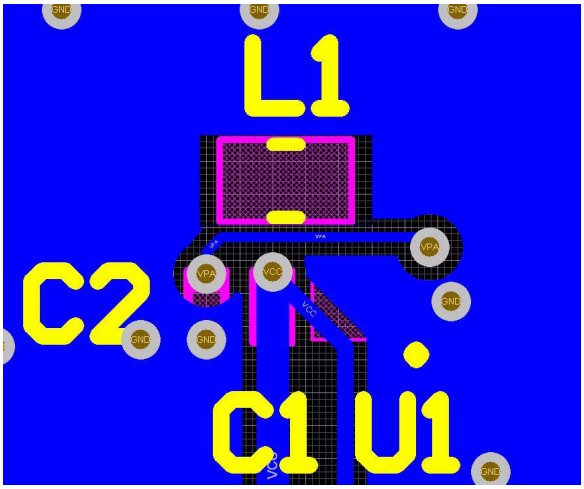
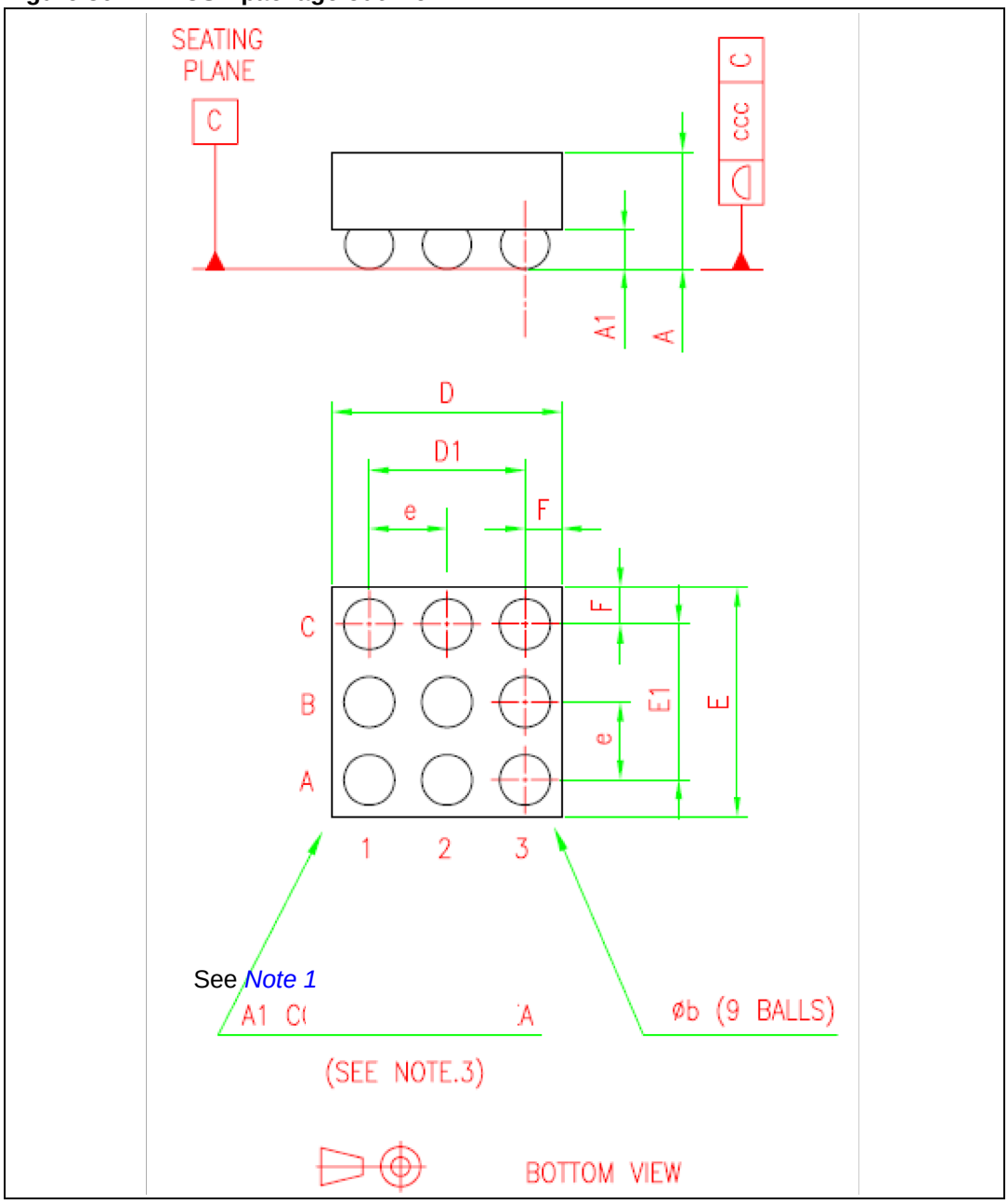


Figure 29. Layer 2



7 Package outline assembly

Figure 30. WLCSP package outline



1. The terminal A1 corner must be identified on the top surface by using a laser marking dot.

Table 9. WLCSP package dimensions(1)

Reference	Min	Typ	Max	Unit
A			0.60	mm
A1	0.17			mm
b(2)	0.23	0.26	0.29	mm
D	1.15	1.18	1.21	mm
D1		0.80		mm
E	1.15	1.18	1.21	mm
F		0.19		mm
ccc			0.05	mm

1. WLCSP stands for Wafer Level Chip Scale Package
2. The typical ball diameter before mounting is 25 mm

8 Ordering information

Table 10. Ordering information

Order code	Package	Packing
PM3110-AW1T	WLCSP 1.2 mm x 1.2 mm	Tape and reel

9 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-May-2010	1	Initial release.
19-Oct-2010	2	Figure updates
29-Jun-2011	3	Updates to final version. Added *Chapter 8: Ordering information*
07-Nov-2011	4	Updated the package height on the cover page.
08-Nov-2011	5	Updated the package height in *Chapter 1: Pin description*
30-Apr-2012	6	Updated the document confidentiality level to “Public”, so it can be published on the company website. No changes in the document content.